Fig.1

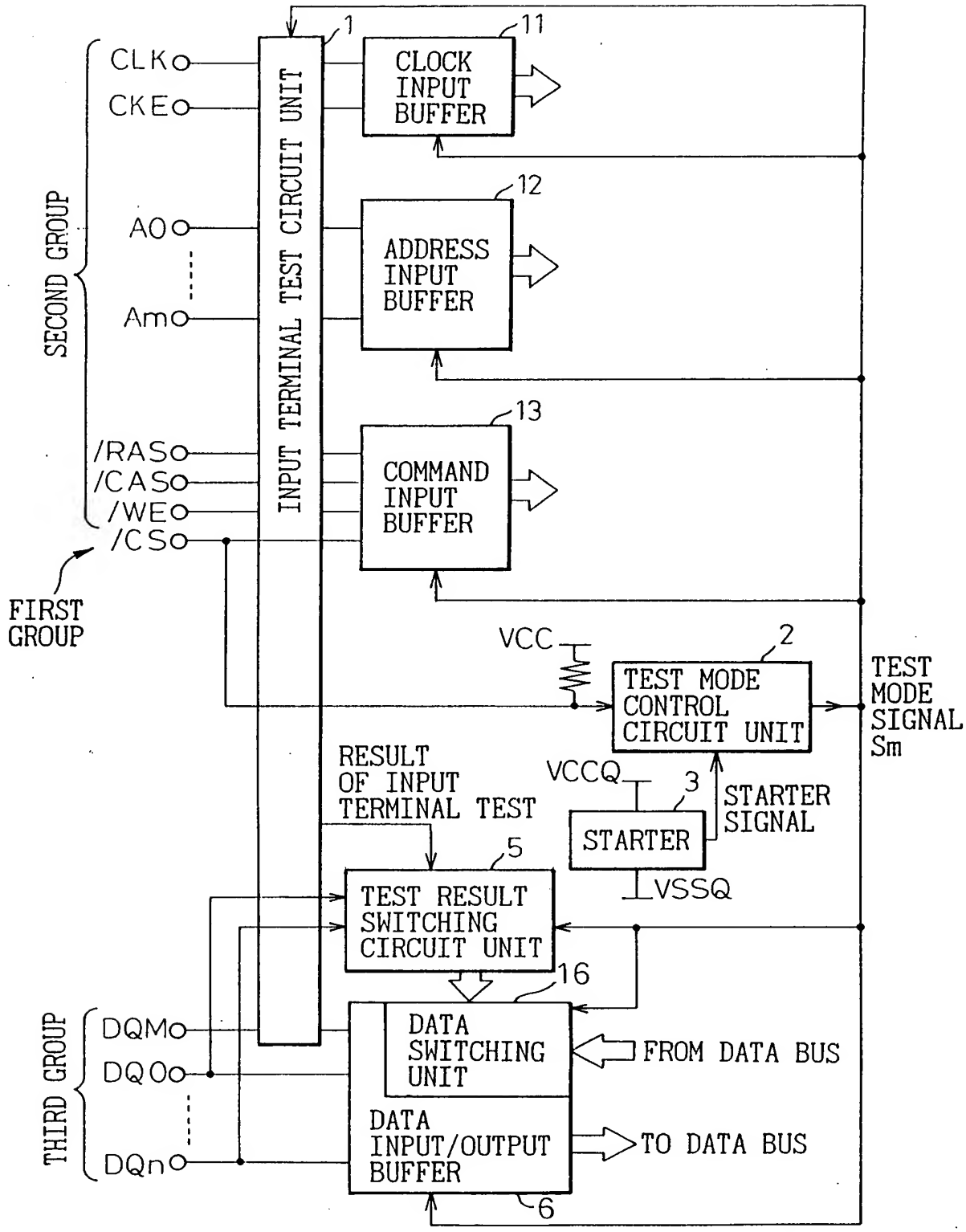

CLK
CKE
A0
Am
/RAS
/CAS
/WE
/CS
SECOND GROUP
FIRST GROUP
INPUT TERMINAL TEST CIRCUIT UNIT
1
CLOCK INPUT BUFFER
11
ADDRESS INPUT BUFFER
12
COMMAND INPUT BUFFER
13
VCC
TEST MODE CONTROL CIRCUIT UNIT
2
TEST MODE SIGNAL Sm
RESULT OF INPUT TERMINAL TEST
VCCQ
3
STARTER
STARTER SIGNAL
VSSQ
TEST RESULT SWITCHING CIRCUIT UNIT
5
16
DQM
DQ0
DQn
THIRD GROUP
DATA SWITCHING UNIT
FROM DATA BUS
DATA INPUT/OUTPUT BUFFER
TO DATA BUS
6

Fig.2

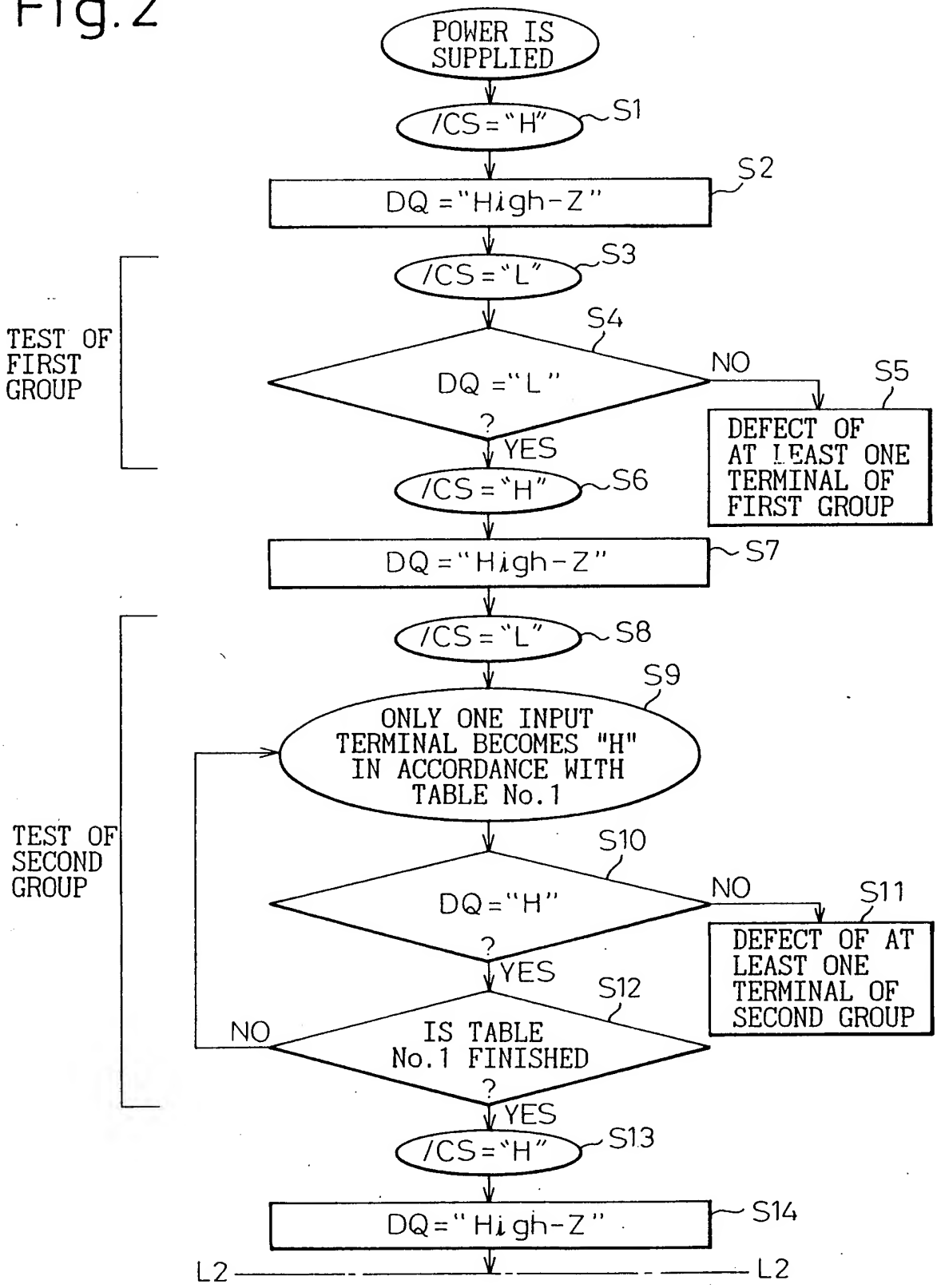

POWER IS SUPPLIED
/CS="H"
S1
DQ="High-Z"
S2
/CS="L"
S3
TEST OF FIRST GROUP
S4
DQ="L" ?
NO
S5
DEFECT OF AT LEAST ONE TERMINAL OF FIRST GROUP
YES
/CS="H"
S6
DQ="High-Z"
S7
/CS="L"
S8
S9
ONLY ONE INPUT TERMINAL BECOMES "H" IN ACCORDANCE WITH TABLE No.1
TEST OF SECOND GROUP
S10
DQ="H" ?
NO
S11
DEFECT OF AT LEAST ONE TERMINAL OF SECOND GROUP
YES
S12
NO
IS TABLE No.1 FINISHED ?
YES
/CS="H"
S13
DQ="High-Z"
S14
L2
L2

Fig.3

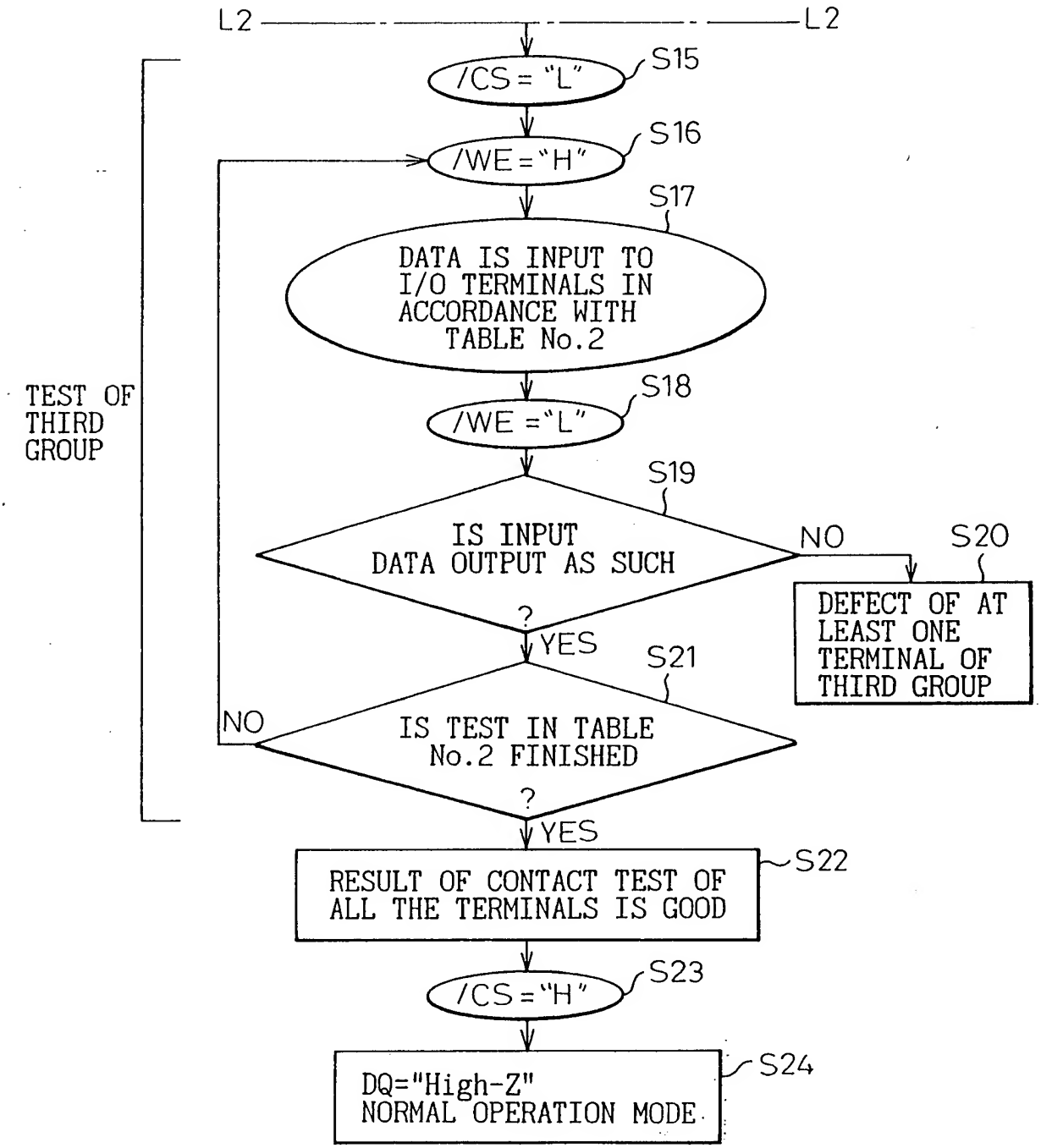

L2
L2
/CS = "L"
S15
/WE = "H"
S16
S17
DATA IS INPUT TO I/O TERMINALS IN ACCORDANCE WITH TABLE No.2
/WE = "L"
S18
S19
IS INPUT DATA OUTPUT AS SUCH ?
NO
S20
DEFECT OF AT LEAST ONE TERMINAL OF THIRD GROUP
YES
S21
NO
IS TEST IN TABLE No.2 FINISHED ?
YES
TEST OF THIRD GROUP
RESULT OF CONTACT TEST OF ALL THE TERMINALS IS GOOD
S22
/CS = "H"
S23
DQ="High-Z"
NORMAL OPERATION MODE
S24

Fig.4

TABLE No.1

TEST INPUT													TEST OUTPUT
A6	A5	A4	A3	A2	A1	A0	DQM	/WE	/CAS	/RAS	CKE	CLK	DQ
0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	0	1
0	0	0	0	0	0	1	0	0	0	0	0	0	1
0	0	0	0	0	1	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0	0	0	1
ANY OTHER INPUT													0

Fig.5

TABLE No.2

TEST INPUT/OUTPUT							
DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
1	1	1	0	0	0	0	0
0	0	0	1	1	0	0	0
1	0	0	1	0	1	1	0
1	1	0	0	1	1	0	0
0	1	0	1	0	1	0	1

REMARKS)
IN THIS CASE, INPUT DATA IS OUTPUT AS SUCH

Fig.6

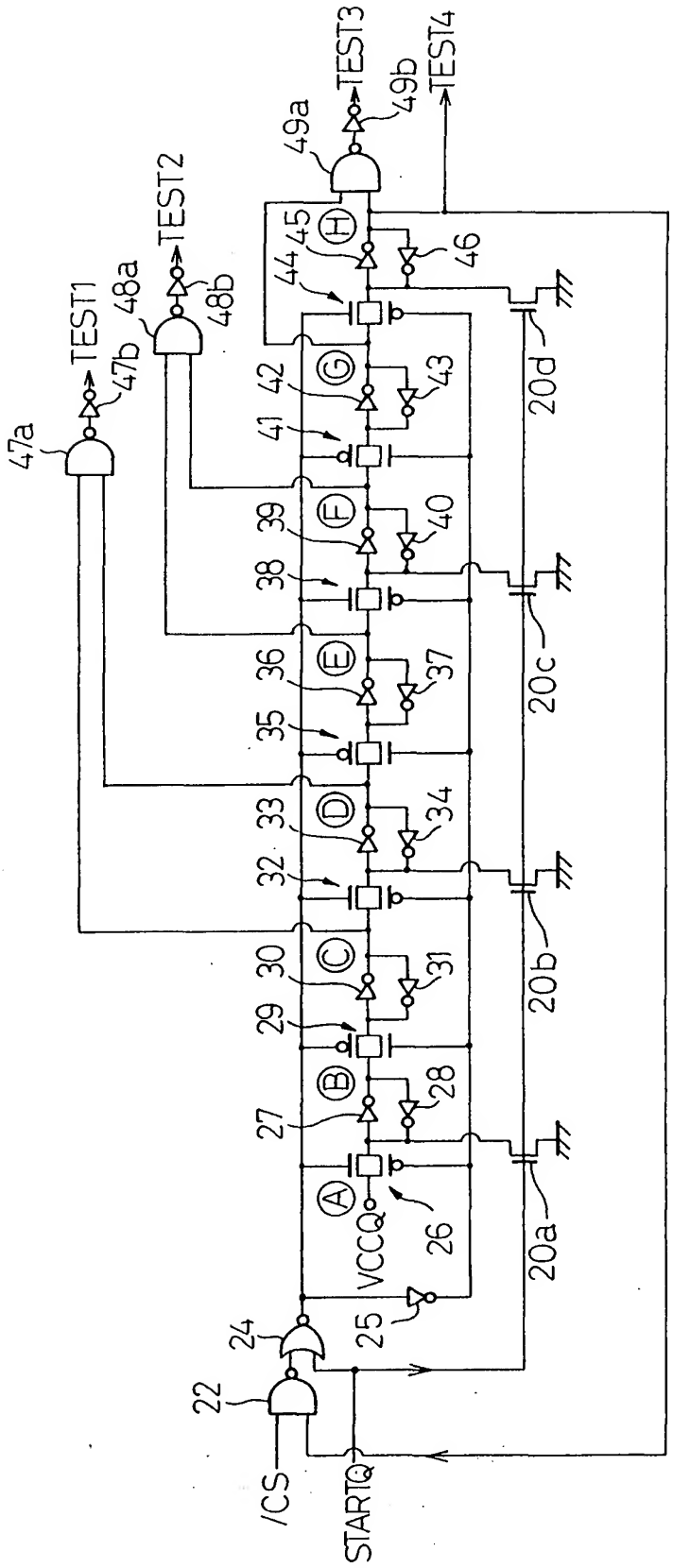

TEST1
TEST2
TEST3
TEST4
47a
47b
48a
48b
49a
49b
/CS
STARTQ
VCCQ
20a
20b
20c
20d
22
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
A
B
C
D
E
F
G
H

Fig.7

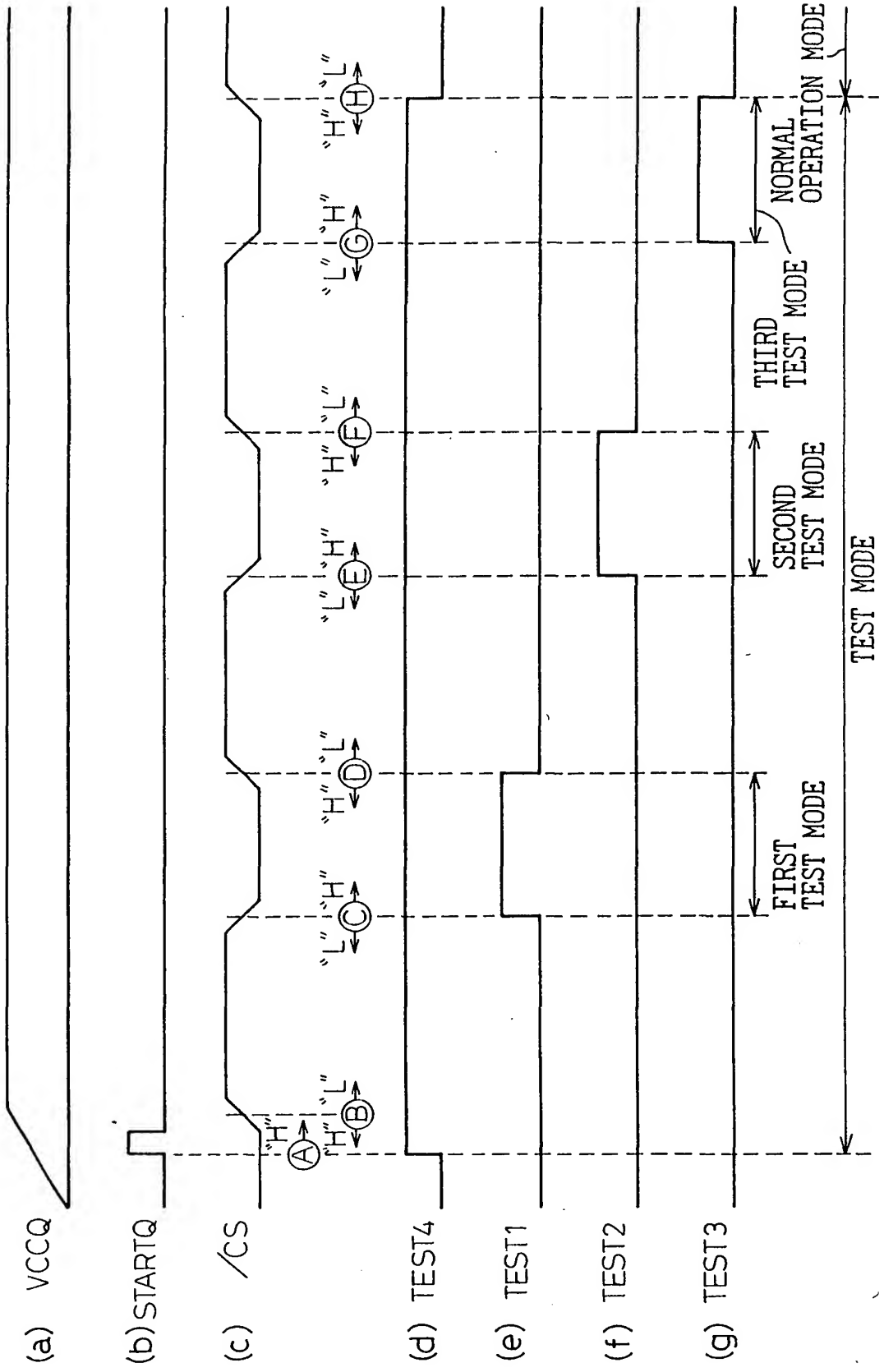

(a) VCCQ
(b) STARTQ
(c) /CS
(d) TEST4
(e) TEST1
(f) TEST2
(g) TEST3
"H"
"L"
A
B
C
D
E
F
G
H
FIRST TEST MODE
SECOND TEST MODE
THIRD TEST MODE
NORMAL OPERATION MODE
TEST MODE

Fig.8

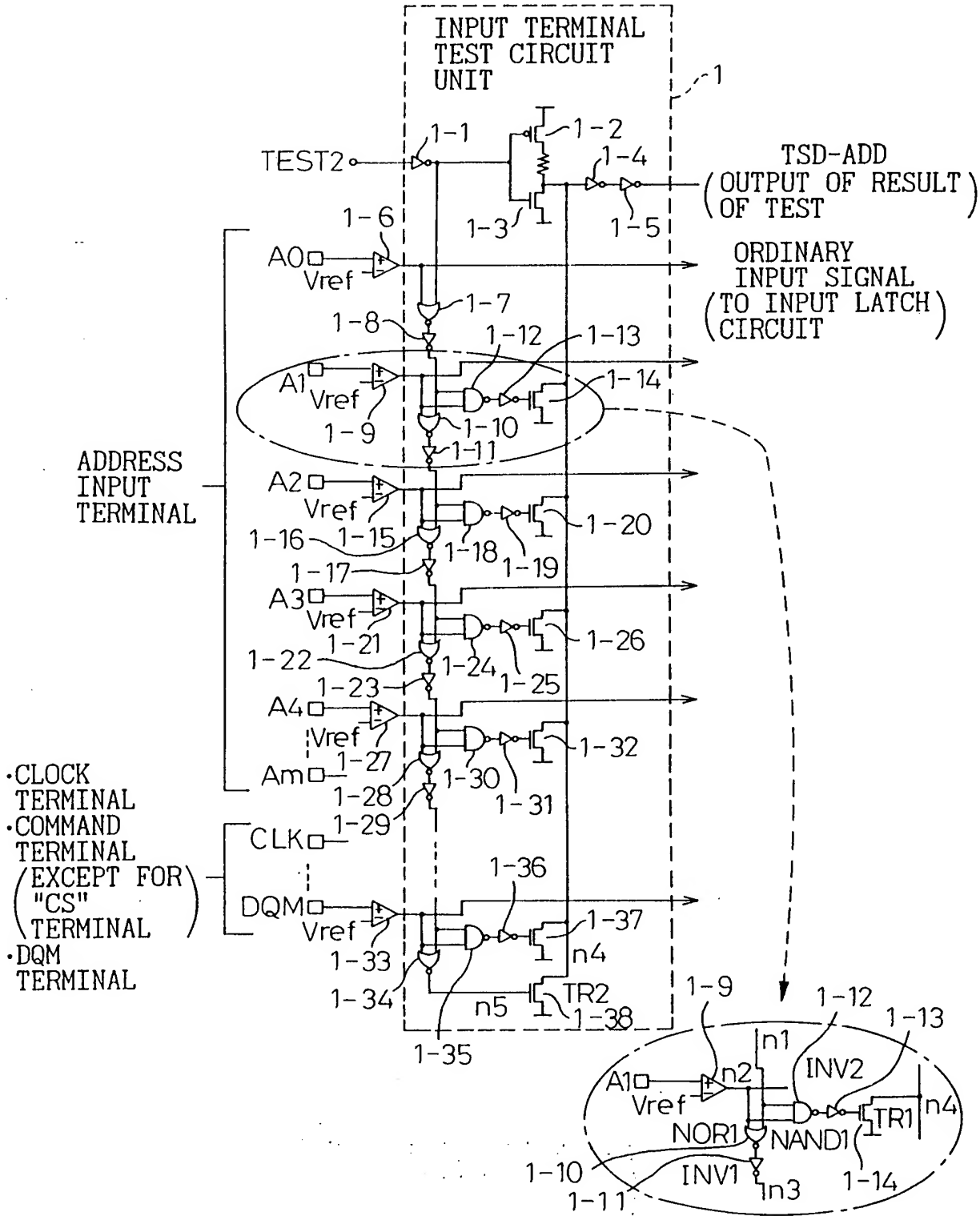

INPUT TERMINAL TEST CIRCUIT UNIT
1
TEST2
1-1
1-2
1-3
1-4
1-5
TSD-ADD (OUTPUT OF RESULT OF TEST)
1-6
A0
Vref
ORDINARY INPUT SIGNAL (TO INPUT LATCH CIRCUIT)
1-7
1-8
1-12
1-13
A1
Vref
1-9
1-10
1-11
1-14
ADDRESS INPUT TERMINAL
A2
Vref
1-16
1-15
1-18
1-19
1-20
1-17
A3
Vref
1-21
1-22
1-24
1-25
1-26
1-23
A4
Vref
1-27
Am
1-28
1-30
1-31
1-32
1-29
·CLOCK TERMINAL
·COMMAND TERMINAL (EXCEPT FOR "CS" TERMINAL)
·DQM TERMINAL
CLK
1-36
DQM
Vref
1-33
1-34
1-37
n4
n5
TR2
1-38
1-35
1-9
1-12
1-13
n1
A1
Vref
n2
INV2
TR1
n4
NOR1
NAND1
1-10
1-11
INV1
n3
1-14

Fig.9

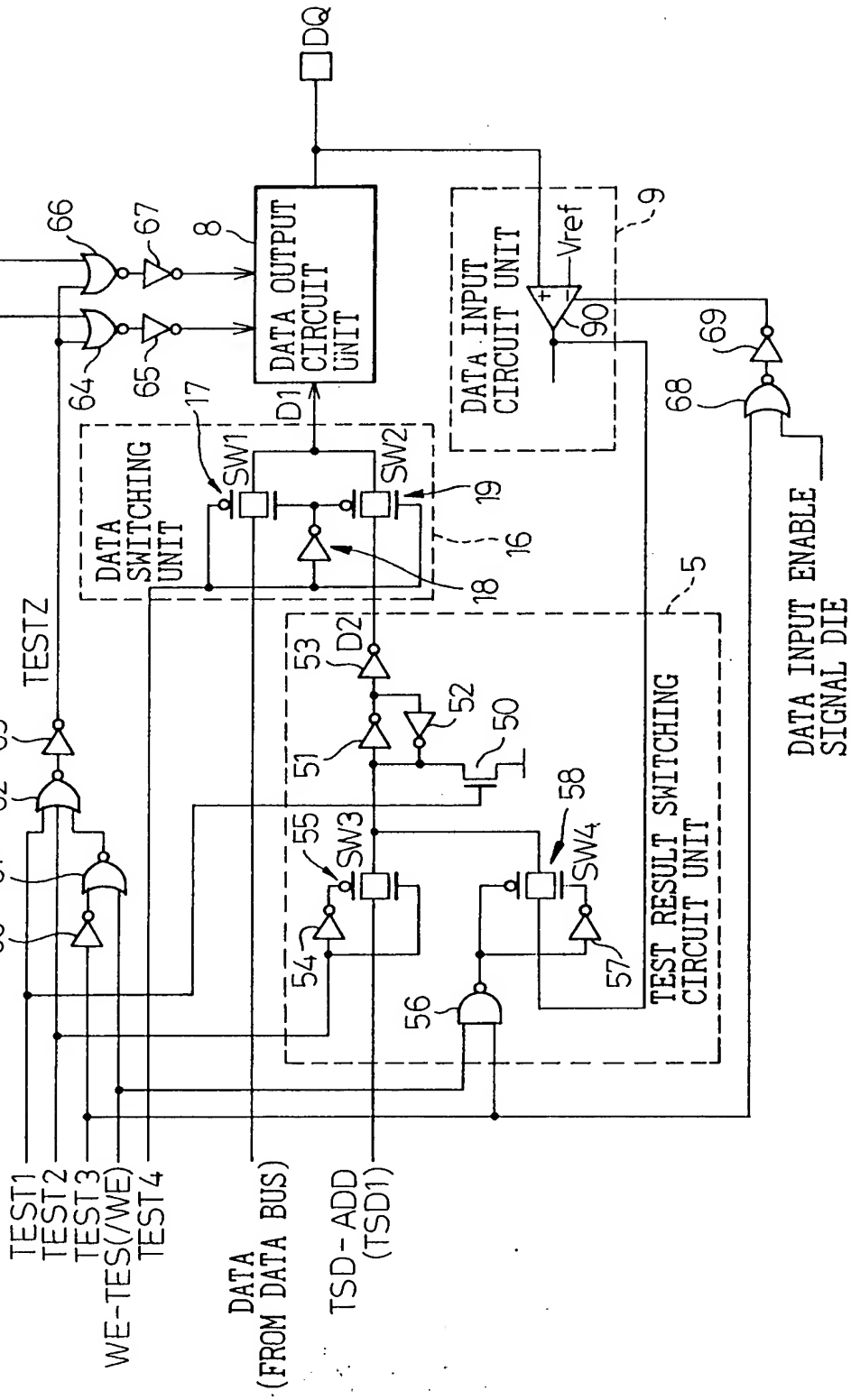
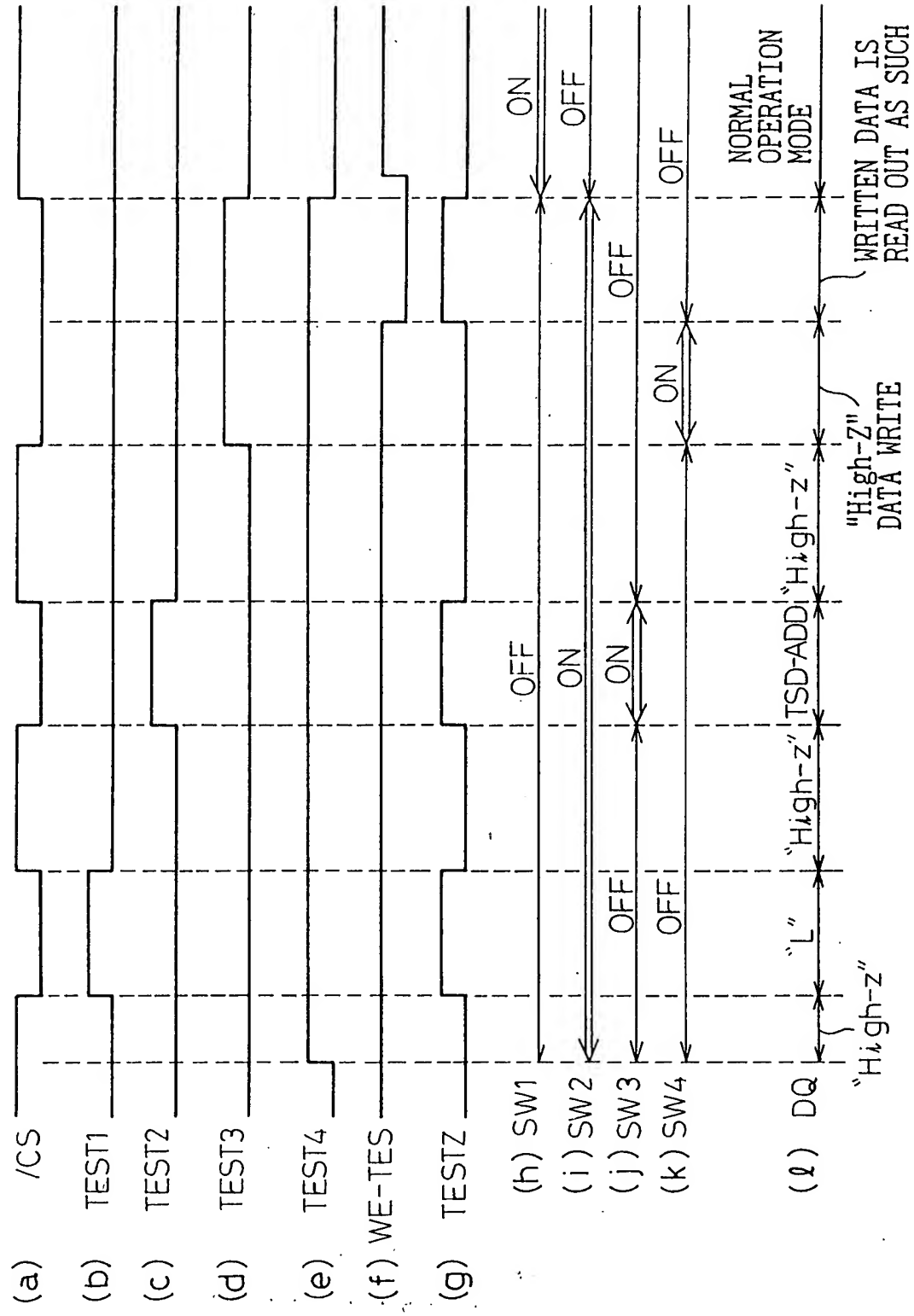

DQ
OUTPUT ENABLE SIGNAL DOE
CLK
66
67
8
DATA OUTPUT CIRCUIT UNIT
64
65
D1
17
DATA SWITCHING UNIT
SW1
SW2
19
16
18
DATA INPUT CIRCUIT UNIT
Vref
9
90
69
68
DATA INPUT ENABLE SIGNAL DIE
5
TEST RESULT SWITCHING CIRCUIT UNIT
TEST2
63
62
61
60
53
D2
52
50
51
58
55
SW3
SW4
54
57
56
TEST1
TEST3
WE-TES(/WE)
TEST4
DATA (FROM DATA BUS)
TSD-ADD (TSD1)

Fig.10


(a) /CS
(b) TEST1
(c) TEST2
(d) TEST3
(e) TEST4
(f) WE-TES
(g) TESTZ
(h) SW1
(i) SW2
(j) SW3
(k) SW4
(l) DQ
ON
OFF
OFF
ON
OFF
ON
OFF
ON
OFF
"L"
"High-z"
TSD-ADD
"High-z"
"High-z"
NORMAL OPERATION MODE
WRITTEN DATA IS READ OUT AS SUCH
"High-Z" DATA WRITE

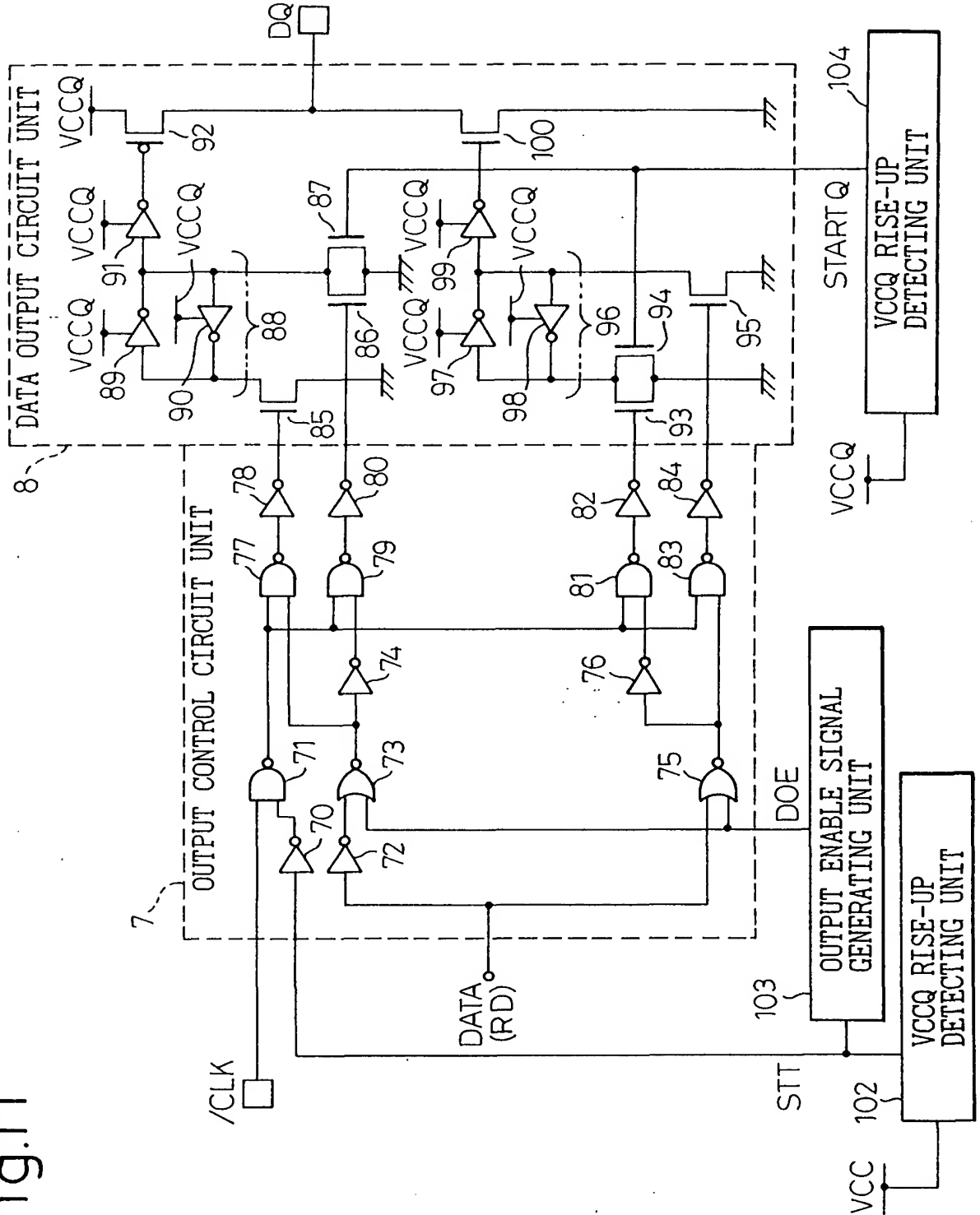

DQ
DATA OUTPUT CIRCUIT UNIT
VCCQ
92
91
89
90
88
87
86
85
100
99
97
98
96
94
95
93
START Q
VCCQ RISE-UP DETECTING UNIT
104
VCCQ
8
OUTPUT CONTROL CIRCUIT UNIT
78
80
77
79
82
84
81
83
74
76
71
73
75
70
72
7
DOE
OUTPUT ENABLE SIGNAL GENERATING UNIT
103
DATA (RD)
/CLK
STT
VCCQ RISE-UP DETECTING UNIT
102
VCC

Fig.11